REMARKS/ARGUMENTS

This application has been carefully reviewed in light of the Office Action dated April 27, 2005. Claims 1-19 remain in this application. Claims 1 and 7 are the independent claims. Claims 1, 7-8, and 12 have been amended. Claims 20-36 have been cancelled, without prejudice. It is believed that no new matter is involved in the amendments or arguments presented herein. Reconsideration and entrance of the amendment in the application are respectfully requested.

Allowable Subject Matter

Claim 12 was indicated to be allowable if rewritten in independent form to include the limitations of the base claim and any intervening claims. Applicant thanks the Examiner and formally recognizes the allowable subject matter of Claim 12.

Specification Objections

The specification was objected to for not having a descriptive title. In response, the title has been amended in accordance with the Examiner's suggestions. Reconsideration and withdrawal of the above objections are respectfully requested.

Drawing Objections

The drawings were objected to under 37 CFR 1.84(p)(5) for failing to mention reference character 84 in FIG. 13 in the description. However, in response, the specification discloses, on page 20, line 22, in reference to FIG. 13, that the semiconductor chips 70 may be bonded by using an adhesive material 84. Thus, the original specification complies with 37 CFR 1.84(p)(5) by mentioning reference

character 84 in reference to FIG. 13 in the description. Reconsideration and withdrawal of the above objections are respectfully requested.

The drawings were objected to under 37 CFR 1.83(a) for failing to show every feature of the invention specified in the claims. However, in response, FIGS. 13-17 illustrate that the second conductive layer 90 has a portion extending in a direction parallel to the stacking direction of the semiconductor chips 70. Reconsideration and withdrawal of the above objections are respectfully requested.

Art-Based Rejections

Claims 1-11, 13, and 19 were rejected under 35 USC §102(b) over USPN 5,571,754 (Bertin); Claims 14-18 were rejected under §103(a) over Bertin in view of USPN 5,973,392 (Senba) and in further view of USPN 6,730,596 (Fukunaga). In response, Applicant respectfully traverses these rejections and submits that the claims herein are patentable in light of the clarifying amendments above and the arguments below.

The Bertin Reference

Bertin is directed to an endcap chip disposed at the top and/or bottom of a multichip stack. *(See Bertin; Figure 12, Ref. Char. 102, 104).* The endcap chip is manufactured by providing a wafer, forming a trench in the wafer, forming a conductive layer in the trench, and separating the endcap chip by polishing the base of the wafer to the bottom of the trench. The conductive layer disposed on the trench forms the conductive layer on the edge of the endcap chip. *(See Bertin; Col. 3, lines 34-52).*

The Senba Reference

Senba is directed to a three-dimensional memory module incorporating a chip-select chip. *(See Senba; Col. 1, line 66 to Col. 2, line 5).* The three-dimensional memory module includes a plurality of semiconductor device unites. Every adjacent tow of the unites are stack-connected via through-holes by a bump connecting method. Each of the units includes a carrier having a circuit pattern and through-holes connected to the circuit pattern. Each unit further includes at least one semiconductor chip mounted on the carrier such that the semiconductor memory chip is connected to the circuit pattern. At least one chip-select chip is mounted on the carrier such that the chip-select chip can select the memory chips. *(See Senba; Col. 2, lines 6-23).*

The Fukunaga Reference

Fukunaga is directed to a method for forming a fine interconnect in a highly integrated circuit formed on a semiconductor substrate. *(See, Fukunaga; Abstract).* The method includes preparing a substrate having fine recesses formed thereon, dispersing ultrafine particles in a predetermined solvent to produce an ultrafine particle dispersed liquid, supplying the ultrafine particle dispersed liquid to the fine recesses of the substrate, heating said substrate to melt and bond the metal, and chemical mechanical polishing the surface of the substrate to remove an excessively attached metal therefrom. *(See, Fukunaga; Col. 1, lines 51-62).*

The Claims are Patentable Over the Cited References

The present application is generally directed to a method for manufacturing a semiconductor device having stacked semiconductor chips.

Claim 1:

As defined by amended independent Claim 1, a method of manufacturing a semiconductor device includes forming a groove on a first surface of a semiconductor

substrate with a plurality of integrated circuits and electrodes being formed on the first surface. An insulating layer is formed on an inner surface of the groove. A first conductive layer is formed on the insulating layer on the inner surface of the groove. A second surface of the semiconductor substrate opposite to the first surface is grinded until the groove is exposed to divide the semiconductor substrate into a plurality of semiconductor chips each of which has a first conductive layer exposed on a side surface of each of the semiconductor chips. A sheet is provided over the first surface, and a filler material is provided between the first surface and the sheet. The filler material is formed integrally over the first surface and in the groove. The semiconductor chips are stacked, and the first conductive layer of one of the semiconductor chips is electrically connected with the first conductive layer of another one of the semiconductor chips.

The applied references do not disclose or suggest the above features of the present invention as defined by amended independent Claim 1. In particular, the applied references do not disclose or suggest, "a sheet being provided over the first surface and a filler material being provided between the first surface and the sheet, and the filler material being formed integrally over the first surface and in the groove," as required by amended independent Claim 1.

Bertin discloses a wafer 10 having trenches 12 etched therein. *(See Bertin; FIG. 1; Col. 5, lines 12-13).* A blanket passivation layer 14 is formed, and a metal layer 16 is then deposited atop the passivation layer 14. The passivation layer 14 and metal layer 16 conformally reside on the walls of trenches 12. *(See Bertin; FIGS. 2-3; Col. 5, lines 46-52).* To protect the metal within trenches 12 and to prevent entrapping of undesired material/chemicals, the trenches 12 are preferably filled with a material 18 which can be subsequently removed. *(See Bertin; FIG. 4; Col. 5, lines 59-62).* A passivation layer 20 is blanket deposited. *(See Bertin; FIG. 5;*

Col. 6, lines 5-6). The lower surface of wafer 10 is polished until substrate 10 is thinned to the trenches 12. Thereafter, material 18 is removed from the trenches 12, and the endcap chips are separated from the wafer 10. *(See Bertin; FIG. 6; Col. 6, lines 10-14).* According to Bertin, material 18 is removed. Moreover, Bertin does not disclose or suggest forming a sheet of material provided over substrate 10 for retaining the separated chips or substrates 10 together after polishing.

In contrast, the present invention discloses that a sheet of material is deposited over the first surface of the substrate with a filler being provided between the sheet and the substrate, as required by amended independent Claim 1 of the present invention. According to the present invention, the sheet 60 is a retaining member for the semiconductor substrate 10. *(See Specification; FIGS. 9-11; page 17, lines 16-20).* As shown in FIG. 9, filler material 62, such as a resin, is provided between the sheet 60 and the substrate 10. The sheet 60 retains the substrate 10 through the filler material 62. At least the groove 30 of the substrate 10 is filled with the filler material 62, and the filler material 62 may be applied to the substrate 10 from the first surface 20 before causing the sheet 60 to adhere to the substrate 10. The filler material 62 may be provided to the sheet 60 in advance, and the groove 30 may be filled with the filler material 62 by causing the sheet 60 to adhere to the substrate 10. *(See Specification; page 18, lines 3-11).* Since the sheet 60 adheres to the substrate 10 on the first surface 20, the divided semiconductor chips 70 can be retained collectively. Thus, handling of the divided semiconductor chips 70 can be facilitated. *(See Specification; page 18, lines 23-25).* Bertin does not disclose or suggest these features of the present invention.

Claim 7:

Claim 7 has been amended in independent form to include the subject matter of base Claim 1. As defined by amended independent Claim 7, a method of

manufacturing a semiconductor device includes forming a groove on a first surface of a semiconductor substrate. A plurality of integrated circuits and electrodes are formed on the first surface. An insulating layer is formed on an inner surface of the groove. A first conductive layer is formed on the insulating layer on the inner surface of the groove. A second surface of the semiconductor substrate opposite to the first surface is grinded until the groove is exposed to divide the semiconductor substrate into a plurality of semiconductor chips each of which has a first conductive layer exposed on a side surface of each of the semiconductor chips. The semiconductor chips are stacked, and the first conductive layer of one of the semiconductor chips is electrically connected with the first conductive layer of another one of the semiconductor chips. At least one insulating substrate is provided between the semiconductor chips.

On page 6, the Office Action purports that Bertin discloses the subject matter of Claim 7, wherein Bertin discloses providing a passivation layer 20 between the semiconductor chips. *(See Bertin; FIGS. 7-8 and 12; Col. 6, lines 5-15).* However, this passivation layer 20 is more related to step (b), forming an insulating layer 40, of amended Claim 7. Bertin does not disclose or suggest forming a passivation or insulation layer in step (e) as suggested by the Office Action.

In contrast, as required by amended independent Claim 7 of the present invention, step (e) discloses stacking the semiconductor chips, wherein step (e) includes providing at least one insulating substrate between the stacked semiconductor chips. As shown in FIGS. 16-17, the present invention discloses an insulator 110, such as an insulating substrate for example, inserted or provided between the semiconductor chips 70 when stacked. The insulating substrate 110 prevents or at least reduces the occurrence of a short circuit between the stacked semiconductor chips 70. In one aspect, the insulating substrate 110 may overlap

the entire outer circumference of the semiconductor chip 70, or overlap a part or portion of the outer circumference of the semiconductor chip 70. Moreover, as shown in FIGS. 16-17, the insulating substrate 110 may be provided to project from the side surface of the semiconductor chip 70. This prevents occurrence of a short circuit between the conductive layers 50 disposed on each side (upper and lower sides) of the insulating substrate 110.

In summary, Bertin does not disclose or suggest these features of the present invention as required by amended independent Claims 1 and 7, and neither Senba nor Fukunaga remedy the deficiencies of Bertin. Therefore, since the applied references do not disclose, teach, or suggest the above features of the present invention as required by amended independent Claims 1 and 7, those references cannot be said to anticipate nor render obvious the invention which is the subject matter of amended independent Claims 1 and 7.

Accordingly, independent Claims 1 and 7, as amended, are believed to be in condition for allowance and such allowance is respectfully requested.

The remaining Claims 2-6 and 8-19 depend either directly or indirectly from independent Claims 1 and 7 and recite additional features of the invention which are neither disclosed nor fairly suggested by the applied references and are also believed to be in condition for allowance and such allowance is respectfully requested.

Conclusion

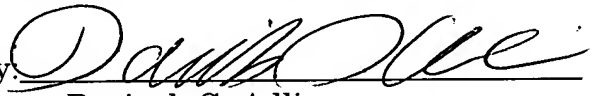
In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6809 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: June 24, 2005

By: 
Dariush G. Adli
Registration No. 51,386
Attorney for Applicant(s)